Research Plan

A Research Proposal Report

On

"Design of a Low Leakage Power Flip Flop with Channel Length Biasing"

Under the supervision of

Prof. P.K.Ghosh
HOD, ECE

10.09.2016

Submitted by

Sumitra Singar
Enrollment. No.
140306

10th September, 2016

Department of ECE, College of Engineering and Technology

Mody University of Science & Technology,

Lakshmangarh, Sikar, Rajasthan-332311

Research plan

Objectives

With the growing uses of portable and wireless electronic systems, reduction in power consumption has become more and more important in today's VLSI circuits. Digital devices like mobile phones, laptops and other portable devices need more battery backup. Hence the power dissipation of these circuits should be as less as possible. High power dissipation also leads to the reduced time of operation, higher weight due to batteries, reduced mobility, cooling cost and reduced reliability. Leakage power has become one of the most critical design concerns for the system level chip designer. While lowered supplies and aggressive clock gating can achieve dynamic power reduction, these techniques increase the leakage power and, therefore, cause its share of total power to increase.

Flip flops are widely used in synchronous sequential digital circuits. In delay flip flop the storing of data get restricted due to leakage current which can limit flip flop from performing its operation. One of the most important state-holding elements is the D-Flip-Flop. Flip flops and latches are bi-stable elements which generally sample its input data continuously whenever an enable input occurs or at a particular time instant defined in term of a clock signal. Delay flip flop stores a particular input pattern and allow processing of it by other parts of digital circuit to obtain complex functions.

In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops, is one of the most power consumption components. It accounts for 30% to 60% of the total system power, where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop. Because of this reason, power consumed by the flip-flops should be as less as possible. Flip-flop is a basic memory element in the digital VLSI design.

Technology scaling increases the density and performance of integrated circuits, resulting in large power dissipations. Low power designs become more and more attractive. The total energy consumption per cycle E_{total} includes three components:

- switching energy E_{sw} : due to charging and discharging for loads,
- short energy E_{short} : due to a direct path from supply voltage to ground, and
- static energy dissipation E_{leak} : that is caused by leakage currents of MOS devices.

The short energy losses can usually be ignored. E_{total} is expressed as:

$$E_{total} = E_{sw} + E_{leakage} = \alpha C_L V_{DD}^2 + V_{DD} I_{leakage} T$$

Performance and energy consumption are equally significant in high-performance and low-power applications. EDP (Energy Delay Product) metric provides a good compromise between delay (t_d) and energy consumption, which is written as:

$$EDP = E_{total} * t_d$$

As supply voltage scales down, the energy consumption reduces and the delay increases. Therefore, the minimum EDP can be reached in a low source voltage.

Here, I will design a low power flip-flop by using the gate-length biasing technique. Gate-length biasing technique is a leakage power reduction technology. Leakage power is the share of total power so reduction in leakage power is the reduction in the total power. Gate length biasing technique reduce two parameters leakage power and Energy Delay Product (EDP). The terms "gate-length biasing" and "L_{Gate} biasing" are used interchangeably to refer to the proposed technique. The phrase "biasing a device" implies adjusting the gate-length of the device slightly. The methodology may be used, to optimize (e.g., reduce) runtime leakage power. Here the use of gate length biasing is based on the goal of reducing leakage power.

The channel length (gate length) biasing technique slightly increases the channel length of transistor to alter the threshold voltage and reduces leakage exponentially. It is reported that small biases in channel length of transistor can afford significant leakage savings with small performance impact. It is well known that leakage power decreases exponentially and delay increases linearly with increasing gate length. Thus, it is possible to increase gate length only marginally to take advantage of the exponential leakage reduction, while impairing performance only linearly. The authors apply gate-length biasing only to those devices that do not appear in critical paths, thus assuring zero or negligible degradation in chip performance. To highlight the value of the technique, the multi-threshold voltage technique, which is widely used for leakage reduction, is first applied and then gate-length biasing is used to show further reduction in leakage. Gate-length biasing is a runtime leakage reduction technique that advantages on the short-channel effect by marginally increasing the gate-length of MOS devices to significantly reduce their leakage current for a small delay penalty. Leakage power is one of the key challenges faced by the semiconductor industry today. Leakage variability is also of great concern and along with timing variability determines the yield.

Leakage current has three main components:

1) sub-threshold leakage,
2) gate leakage and
3) reverse biased drain substrate and source-substrate junction band-to-band tunneling leakage.

Leakage reduction methodologies can be divided into two classes depending on whether they reduce:

1) standby leakage
2) run time leakage.

Standby techniques reduce leakage of devices that are known not to be in operation, while runtime techniques reduce leakage of active devices. Several techniques have been proposed for standby leakage reduction such as body biasing or VTMOS, MTCMOS, source biasing, use of transistor stacks, input vector control, etc. However, very few approaches have been proposed for runtime leakage reduction and threshold-voltage (V_{th}) assignment is the only mainstream

approach. Other recently proposed runtime leakage reduction techniques include gate-length biasing and adaptive body biasing. One advantage of this technique is that small increases in gate-length can have significant effects on device characteristics such as leakage current reduction since they take significant advantage of the SCE and incur only small penalties in drive current and input capacitance. Typically, leakage power decreases exponentially, and delay increases linearly, with increasing gate-length. The gate-length biasing technique of the present invention may be applied as:

1) at the cell level or
2) at the transistor level.

At the cell level, the approach enhances a standard cell library by adding L_{Gate} biased variants to the library. The gate length biasing methodology is applied primarily to devices in non-critical timing paths, to optimize device characteristics. For example, in the context of leakage reduction, a leakage optimization approach is used to incorporate slower, low-leakage cells into non-critical paths, while retaining faster, high-leakage cells in critical paths. On the other hand, at the transistor level, since different transistors control different timing arcs of a cell, gate-length biasing at the transistor level includes individually modifying delays of different timing arcs. Asymmetry in timing criticality of different timing arcs of a cell instance in a circuit, and that of rise and fall transitions, can be used by transistor level gate-length biasing to yield significant leakage savings.

The gate-length biasing (GLB) technology increases the channel length of transistors to alter the threshold voltage and reduces leakage exponentially in both active and standby modes, while delay increases linearly with increasing gate length.EDP (Energy Delay Product) metric provides a good compromise between speed and delay. Multi-threshold voltage designs offer high performance with low runtime and standby leakage power. Low V_{th} devices offer high performance but are leakier. While high V_{th} devices are slow but leak less. Circuit optimization techniques use low V_{th} devices (cells) on critical paths while high V_{th} is used for all other devices (cells). Multiple V_{th}'s are manufactured by altering the doping levels over the diffusion regions in MOS devices. Extra masks and lithography steps are required for achieving multiple V_{th}'s, therefore the process costs increase. The increased costs have been outweighed by the substantial leakage reductions they provide, and dual and triple-V_{th} processes are now standard.

A flip-flop is important element in digital circuits. I am doing work on a low-leakage power flip-flop with gate length biasing (GLB) technology to achieve low energy delay product (EDP) and low leakage power consumption. As we are going from one technology generation to next technology generation as the device size is becoming smaller and smaller, but the leakage power is increasing at a much higher rate, and leakage current is increases at a faster rate than dynamic power in various technology generations and at some point the leakage power will be more than the dynamic power.

Objective

- Design of low leakage power flip flop by using Gate Length Biasing (GLB) technique.
- To achieve low leakage power consumption in VLSI design with minimum power delay product.
- To improve the resource utilization in low power VLSI design by using low leakage techniques.
- Tool to be used: tanner EDA.
- Technology: 45 nm technology.

Gantt Chart

Task\Year	2014	2015	2015	2016	2016	2017	2017
	Aug.-Dec.	Jan.-July	Aug.-Dec.	Jan.-July	Aug.-Dec	Jan.-July	Aug.-Dec
Research Methodology							
Self-study course							
Literature review							
Research topic refinement							
Research gap analysis							
Comprehensive Exam							
Objective Definition							
Paper Published							
Paper publication							
Research work implementation							
Thesis							